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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/677,392	09/29/2000	Aditya Mukherjee	042390.P9572	3111

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EXAMINER
CHAUDRY, MUJTABA M

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/677,392	Applicant(s) MUKHERJEE, ADITYA	
	Examiner Mujtaba K Chaudry	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

The drawings are objected to because:

- This application, filed under former 37 CFR 1.60, lacks formal drawings. Specifically, Figures 1-4 filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

- The abstract is objected to because it is not descriptive of the invention. Applicant is reminded of the proper **content**, **language** and **format** for an abstract of the disclosure.

  The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

  A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of

> ***an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative. The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art. Extensive mechanical and design details of apparatus should not be given.***

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1 lines 6-7, the limitation "at least one design" which is vague and should be amended accordingly without adding new matter. Applicant is to note that independent claims 10 and 18 include similar limitations which need to be addressed as well. Furthermore, claims 2-9, 11-17 and 19-20 are depending from the independent claims and inherently included limitations stated therein, and therefore are rejected as well. For examination purposes the examiner has given the term "one design" its broadest interpretation as directed by the MPEP.

Claims 5-9, 13-17 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicant states in claims 5, 13 and 20 the limitation, "$n = a + \log_2 i$" which is not fully defined. In the equation "n" is defined to be the number of lines, "a" is defined to be number of ancillary transmission bits and "$\log_2 i$" is defined as the number of instruction bits. Applicant defines "$\log_2 i$" in the specification (page 12, line 1) component "i" to be the number of instructional bits. It is contradictory for the instructional bits to be "$\log_2 i$" and "i" because $\log_2 i \neq i$. Furthermore, applicant fails to explicitly define variable "i" in the claim language as required. As a note of reference, dependent claims 6-9 and 14-17 inherently include limitation set forth in the related independent claims 5 and 13 and therefore are rejected accordingly.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wasson (USPN 6181151 B1).

As per claims 1-4, 10-12 and 18, Wasson substantially teaches (title and abstract) an integrated circuit tester with a plurality of tester channels for testing a device under test. The tester channels include an instruction memory for storing a set of test instructions which are executed during testing. Wasson teaches the test instructions to include a vector data which indicates a particular test and other instructions which direct a certain number of data bits to the tester. Wasson teaches (Figure 1 and col. 4, lines 17-54) a host computer which signals a disk controller to read the instructions for the tester channel and write those instructions onto an instruction memory—analogous to memory chip in the present application. The examiner would like to point out that the test controller in the present application is analogous to the disk controller of Wasson, since the test controller (in the present application) is defined to be any device that asserts test instructions (present application: specification page 6, lines 13-17). A test bus is shown in figure 1 (Wasson) that is connected to the test controller/disk controller and the logic unit control. The logic unit controller/deskew controller in the present application is analogous to the timing circuit of Wasson, since the logic unit controller/deskew controller is defined to synchronize the instructions (present application: specification pages 7-8, lines 28 and 1-5 respectively). As regards to the "design" limitation of the present application, Wasson teaches (col. 4, line 30) logic test activities that include various designs. As a note of reference the "design" limitation is also rejected above under 35 USC 112, 2nd paragraph for being indefinite. Wasson teaches (col. 4, lines 17-21) the tester to be adapted to test programmable logic devices which is analogous to logic unit in the present application.

Wasson does not explicitly teach the external device to comprise of a keyboard, mouse and a modem as stated in the present application.

However, Wasson teaches a host computer (figure 2) which is used as control means for the testing apparatus. Specifically, Wasson teaches (col. 4, lines 31-45) the tester to include a host computer which is signals the disk controller to read and write instructions to the instruction memory. Furthermore, the examiner would like to point out that a host computer is defined (The Authoritative Dictionary of IEEE Standard Terms, 7th ed.) to be a computer attached to a network providing primary services such as computation, data base access, special programs or programming languages which may have multiple processing elements (i.e. keyboard, mouse, etc).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate a keyboard, modem and a mouse within the system of Wasson as stated in the present application. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that a host computer might inherently include a keyboard, mouse and modem for communicating with a testing apparatus which would also abate complications involved.

As per claims 5-9, 13-17 and 19-20, Wasson substantially teaches, in view of above rejections, (col. 5, lines 55-68—col. 6, lines 1-42) a set of instruction bits and an instruction memory register as stated in the present application. Specifically, Wasson teaches to supply the instructions to each channel CH(1)-CH(N) before testing and supplying scan data (analogous to ancillary data in the present application) to various channels during a test. Before the start of the test the disk controller reads the channel instructions and writes them into the instruction

memory of each channel. The disk controller also reads control data for each channel out of disk and writes that control data into a set of addressable control registers within the channel via memory bus and memory controller. The control data stored in addressable control registers tells shift register which M bits of the 12-bit scan data word that it is to shift in. If the channel is the only channel using scan data during a test M is 12 and the channels' shift register shifts in all 12 bits of scan data in response to each SHIFT_IN signal pulse. For example if four channels use scan data during a test, the control data tells the shift register of each channel to shift in a particular set of three of the 12 scan data bits. The control data also tells state machine how many scan bits are being shifted in so that state machine knows how many test cycles to wait between successive SHIFT_IN pulses. Wasson teaches (figure 2) a state machine that is analogous to the finite state machine in the present application.

Wasson does not explicitly teach a test bus to include n number of lines such that "$n = a + \log_2 i$" wherein "n" is defined to be the number of lines, "a" is defined to be number of ancillary transmission bits and "$\log_2 i$" is defined as the number of instruction bits as stated in the present application.

However, the examiner would like to point out that Wasson does teach a process that is similar and essentially includes this variation. Specifically, Wasson teaches (col. 6, lines 43-67) to supply control instructions and scan data (analogous to ancillary transmission bits) to each channel before testing. Furthermore the control data determines what number of M bits of the 12-bit scan word will be sent and also how the encoder converts the scan data. The control data also determines tells state machine (analogous to finite state machine in the present application) how many scan bits are being shifted in so that state machine knows how many test cycles to

wait between successive SHIFT_IN pulses (analogous to clock signal for the ancillary transmission bits in the present application).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention was made to define the design parameters of Wasson by setting them in accordance to the equation "$n = a + \log_2 i$" wherein "n" is defined to be the number of lines, "a" is defined to be number of ancillary transmission bits and "$\log_2 i$" is defined as the number of instruction bits as stated in the present application. This modification would have obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that the equation "$n = a + \log_2 i$" (wherein "n" is defined to be the number of lines, "a" is defined to be number of ancillary transmission bits and "$\log_2 i$" is defined as the number of instruction bits) is an obvious design choice that one is entitled to in the making of the method and apparatus. Furthermore, the examiner would like to point out that there are several ways to state a limitation mathematically, which essentially holds the same underlying meaning.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. It is the examiner's conclusion that the invention described in the application is not patentably distinct or non-obvious over the prior art. Wasson teaches an integrated circuit tester with a plurality of tester channels for testing a device under test. Applicant is further invited to read/review additional pertinent prior art that has been appended herein.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 703-305-7755. The examiner may normally be reached Mon – Thur 7:30 am to 4:30 pm and every other Fri 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 703-305-9595. The fax phone number for the organization where this application is assigned is 703-746-7239.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the receptionist at 703-305-3900.

Mujtaba Chaudry
Art Unit 2133
March 5, 2003

ALBERT DECADY
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